Robust Matrix Converter Commutation without explicit Sign Measurement

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Abstract
A new operation method for matrix converters is presented which eliminates the extra measuring circuits of voltage or current signs that were necessary for the commutation in the past. The paper explains the new robust method that minimises switching losses. Advantages and disadvantages of different approaches are discussed and measurements on a 5.5 kW matrix converter system are shown.

Introduction
The matrix converter is discussed academically for more than 20 years. The progress on silicon semiconductors has enabled a great advance on this type of converter making it interesting for industrial usage. The matrix converter is a simple 3 to 3 phase converter (Fig. 1). By using 9 bi-directional switches (BDS) the matrix converter is able to create a variable output voltage system of a desired frequency and magnitude [1-12]. If an ordinary LC-filter is added the grid is stressed by sinusoidal current, only. The converter offers power regeneration and an adjustable input power factor $\cos \phi_i$ with little reduction to the active power transfer ratio. The sinusoidal voltage transfer ratio is limited to 0.86 on principle. A basic problem of the matrix converter is the absence of passive free wheeling paths for the load. This makes the matrix converter hard to handle concerning the commutation behaviour and at pulse-off. A reliable protection and a save commutation strategy has to be found and implemented. This paper deals with the commutation of the matrix converter. The subject of protection can be found in [11, 12].

Commutation styles
The knowledge of the matrix converter commutation is elementary to understand the difficulties of the converter. The commutation process can be studied on a single output phase as it is shown in Fig. 2. In contrast to the well known DC-voltage link converter a commutation cannot be initiated without any knowledge of the commutation conditions. To do a commutation
The evaluation of the sign of the input voltage \( v_{AB} \) but are independent of the current sign. They are named “voltage commutation” and are explained in [1]. The two sequences on the Y-axis do only need the evaluation of the sign of the load current \( i_{\text{load}} \). They are named “current commutation” [3].

The remaining sequences need the evaluation of both signs. This fact makes them harder to handle. As a result, voltage or current commutation should be used.

Additionally, Fig. 3 indicates the switching moment when the commutation actually appears. Natural and forced commutation are distinguished. The kind of commutation can not be influenced and depends on the conditions of the load current and the input voltage at the commutation moment.

Another idea to do a commutation is the “two step commutation”. The basic idea is to switch only the IGBT in a BDS which will lead the load current. In addition, all IGBTs in the matrix which will not conduct are switched on. This will reduce the dead time and is opening additional free wheeling paths for the load current in case of error. The two step commutation can be voltage controlled [5] or current controlled [6]. In the following paper deals with the four step voltage controlled commutation if not commented differently.

**Commutation strategies**

The shown commutation styles have been presented in many papers [1-6, 10]. The general structure of the most used test set-ups is shown in Fig. 4. PWM generator and commutation logic are divided in separate logic devices. The commutation logic deals only with the switching commands of the PWM generator and the utilised sign of commutation. The detection of the sign is done by a special circuit arrangement. The circuit has to work between the maximum
input voltages or load currents. Therefore, this circuit has to stand high demands. It has to be very precise making it expensive. An error in sign detection will lead to a short circuit which may destroy the IGBTs. This has to be prevented. Normally, the sign detection works well and a loss optimised modulation can be used. A loss optimised modulation is switching between voltages that do not differ much from each other. In the marked uncritical area in Fig. 5 a switching sequence can be $B \rightarrow C \rightarrow A$ and backwards. A critical situation appears if two voltages of the input phases become equal.

There are several possibilities to manage a critical situation of commutation if no precise sign detection is desired:

- **Prohibition:** A critical commutation sequence is not executed until the voltages differ enough from each other (or the current sign can be detected without failure concerning the current commutation [4]). The effect on the output is little because the voltages have a small difference. A disadvantage is the shape of the input current. Because of the calculated pulse patterns which will not be executed the input current will differ from the ideal sinusoidal shape.

- **Evaluation of current and voltage sign:** A combination of voltage and current commutation may help in a lot of cases. The sequences used can be chosen from Fig. 3. Before a sequence is initiated the signs and their reliability are checked. Finally, there will be situations in which both signs are unsure. As a result the method as described in “prohibition” has to be chosen.

- **Replacement:** A critical area is driven around (Fig. 6). The critical sequence is replaced by two uncritical sequences which will commutate to the remaining third input phase and then to the desired destination phase. This method is described in [7] for a two step commutation. It fits for four step commutation, too. The method is effective and easy to implement in the commutation logic. Only an information about a critical area has to be added. A disadvantage is caused by the extra sequences which are inserted. They will increase the switching losses of the converter. In non-critical areas the modulation can be executed without insertion of additional sequences.

- **Prevention:** A new idea is to avoid the critical switching patterns in a critical area (Fig. 7). This new method has been found by using the “Rectifying and Inverting Vector Modulation”

![Fig. 5: Critical areas of commutation sequence selection](image)

![Fig. 6: Insertion of two additional sequences to phase C in a modulation period at a critical area between phase A and B with method “replacement”](image)

![Fig. 7: Rearrangement of the modulation patterns in a modulation period at method “prevention”](image)
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In a critical area the modulation patterns are reshuffled that way that no critical sequence appears. No additional sequences are required compared to the “replacement” method. In the following this method is described more detailed.

Robust method “prevention”

The strategy of this method is simple and easy to implement. Fig. 7 shows the same demanded average output voltage as in Fig. 6. The modulation patterns demanded by the PWM are rearranged. Instead of using the sequence “A→B→C” the critical step from phase A↔B is avoided by rearranging the sequence to “A→C→B”. Neither the average value of input current is influenced nor the average value of the output voltage. To implement this method the system structure has to be modified. An example is given in Fig. 8. The difference to the former structure is the connection of the A/D-converters. Normally, the A/D-converters are read out directly by a digital signal processor (DSP) or a micro controller (MC). The resolution of the voltage signal is limited to the sampling time of the processor. To do the normal PWM a sampling time of 100 µs to 50 µs is enough. To replace an exact sign detection circuit the resolution in time of the A/D-converters has to be increased. The increase of the sampling time of the processor can be a solution but is an expensive way. Another way is to implement the PWM generator, the commutation logic, the sign detection and A/D-converter control in one logic device (e.g. Field Programmable Gate Array FPGA). Now, the voltage signal can be sampled independently from the demands of the PWM generation. If a sigma-delta-converter is used the measured bit stream has to be filtered to analyse the value of the input voltage. From the voltage signal the critical and uncritical areas and the voltage signs are calculated. The sampling rate of the sigma-delta-A/D-converter and the necessary size of the critical area are related. A window which characterises the critical area in the input voltage system has to be defined. The window with the borders of a critical voltage level $V_{\text{crit}}$ has to be chosen that way that an disturbed input voltage can not have any influence on the commutation process. The worst case of this assumption is an excitation of the L-C-filter at the input lines of the converter, e.g. at power turn on of the converter. The values of the filter devices are well-known and the resonant frequency can be calculated from the formula:

$$f_{\text{res}} = \frac{1}{2\pi \cdot \sqrt{L_C \cdot C_F}}$$

(1)

Having a look at Fig. 10 a short circuit of the input voltage sources can only happen if a disturbed phase-to-phase voltage with a zero crossing is not detected within a certain time and the modulator is not switched to the method “prevention”. By knowledge of the resonant frequency $f_{\text{res}}$ and a maximum assumed voltage magnitude $\hat{v}_{\text{res}}$ of the oscillating filter a maximum time of conversion $t_{\text{Max}}$ at excitation can be determined. A linearization of the grid

Fig. 9: Signal structure of the new sign detection rate of the sigma-delta-A/D-converter and the necessary size of the critical area are related. A window which characterises the critical area in the input voltage system has to be defined. The window with the borders of a critical voltage level $V_{\text{crit}}$ has to be chosen that way that an disturbed input voltage can not have any influence on the commutation process. The worst case of this assumption is an excitation of the L-C-filter at the input lines of the converter, e.g. at power turn on of the converter. The values of the filter devices are well-known and the resonant frequency can be calculated from the formula:

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Fig. 10: Zero crossing of the phase-to-phase input voltage (50Hz) with filter resonance of 20% $\hat{v}_{N}$ at 1.7 kHz
sinus and the resonant sinus graph with no phase shift will lead to:

\[ t_{\text{Max}} = \frac{V_{\text{crit}}}{2\pi \cdot (f_N \cdot \hat{v}_N + f_{\text{res}} \cdot \hat{v}_{\text{res}})} \]  

(2)

In which \( f_N \) and \( \hat{v}_N \) are the grid frequency and the maximum magnitude of the phase-to-phase input voltage. The maximum gradient exists at zero crossing of the phase-to-phase input voltage. Fig. 10 shows this situation with a superimposed 1.7 kHz oscillation of the L-C-filter with a magnitude of \( \hat{v}_{\text{res}} = 20\% \cdot \hat{v}_N \). The grid was assumed to:

\[ v_{N(t)} = 566 \text{V} \cdot \cos (2\pi \cdot 50 \text{Hz} \cdot t) \]

According to the delay time of the A/D-conversion and the processing time of the digital filters a dead time \( t_d \) has to be considered. The tolerant time of conversion \( t_T \) is:

\[ t_T = t_{\text{Max}} - t_d \]  

(3)

Now, the maximum permissible magnitude of a disturbance by excitation can be calculated from:

\[ \frac{\hat{v}_{\text{res}}}{\hat{v}_N} = \frac{V_{\text{crit}} \cdot 1}{\hat{v}_N \cdot \frac{\pi}{2} \cdot (t_T + t_d) \cdot f_{\text{res}}} \]  

(4)

Table I gives a few examples for the reduced time of conversion of the new method. The resonant frequency of the filter was assumed to \( f_{\text{res}}=1.7 \text{ kHz} \) again.

<table>
<thead>
<tr>
<th>( V_{\text{crit}} ) (V)</th>
<th>( \hat{v}_{\text{res}} / \hat{v}_N )</th>
<th>( t_d ) (µs)</th>
<th>( t_T ) (µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>20 %</td>
<td>4</td>
<td>32</td>
</tr>
<tr>
<td>50</td>
<td>40 %</td>
<td>8</td>
<td>11.26</td>
</tr>
<tr>
<td>50</td>
<td>80 %</td>
<td>8</td>
<td>1.97</td>
</tr>
<tr>
<td>50</td>
<td>100 %</td>
<td>10</td>
<td>( \times )</td>
</tr>
<tr>
<td>100</td>
<td>20 %</td>
<td>4</td>
<td>68.1</td>
</tr>
<tr>
<td>100</td>
<td>40 %</td>
<td>8</td>
<td>30.5</td>
</tr>
<tr>
<td>100</td>
<td>80 %</td>
<td>8</td>
<td>11.94</td>
</tr>
<tr>
<td>150</td>
<td>80 %</td>
<td>4</td>
<td>21.91</td>
</tr>
<tr>
<td>150</td>
<td>100 %</td>
<td>10</td>
<td>14.1</td>
</tr>
</tbody>
</table>

Table I: Examples of tolerant time of reaction for sign detection

The case marked with \( \times \) can not be handled with a causal system because the time \( t_T \) becomes negative. That means the PWM has to be switched to “prevention” before the voltage is detected. That shows, the capability of the new voltage sign detection of the matrix converter is limited by the characteristics of the used signal processing. An additional aspect is the measuring accuracy of the A/D-converters and additional disturbance of the input voltage caused by higher harmonics of the grid. To avoid an error in voltage sign detection the window marking the critical area should be selected carefully. A good security distance is recommendable.

Investigations on an experimental set-up (Fig. 11) have shown that a window for critical area should be chosen to 20-27% of \( \hat{v}_N \). For
example, the window for input phase A & B should be defined to:

\[ |V_{\text{crit}}| \leq 0.25 \cdot \hat{V}_N \]

The time of “prevention” modulation is about 38-50% of the main period.

The same timing considerations as presented for the method “prevention” can be used for the method “replacement”. An advantage of “replacement” is that it works by detection of the critical area. At method “prevention” a problem occur if the critical area is detected within a modulation period. A started sequence can not be reshuffled (Fig. 14). The method “replacement” can work as a final instance. The combination of both methods is perfect to a robust commutation without sign measurement.

**Experimental test set-up**

The new commutation method has been developed and tested on a 5.5 kW matrix converter test set-up as shown on Fig. 11. The BDS are collector connected IGBTs which are all placed in a single ECONOMAC chase of EUPEC [13]. This will ensure a compact design of the set-up and a low parasitic stray inductance from the filter capacitors to the IGBTs. The filter capacitors are connected in delta configuration. The 3-phase filter coils can be seen on the left side of the picture. The two PCB boards contain the gate units, A/D-converters and the over-voltage protection circuits. The system is controlled by a TMS320C40 DSP system. The FPGA containing PWM generator, commutation logic and sign detection are implemented in an EPF 10K100 device from Altera. The methods “prevention” and “replacement” are realised.

**Measurements**

Fig. 12 & 13 show the input and output voltages and currents of the matrix converter set-up at a passive R-L-load at standard operation. The matrix converter is able to adjust its input power factor. This feature has been implemented in the set-up. The power factor has been corrected to one to compensate the capacitive characteristic of the input filter. Fig. 14 shows the change of the PWM algorithm from a loss optimised modulation to

![Grid voltage and grid current of the matrix converter](image1)

**Fig. 12**: Grid voltage and grid current of the matrix converter

![Load voltage and load current at a passive R-L-load](image2)

**Fig. 13**: Load voltage and load current at a passive R-L-load

a step of the “replacement” method and then to the method of “prevention”. The combination of the two methods works perfect. After the critical area is passed a loss optimised modulation is used, again. To verify the robustness of the prevention method the converter was tested under a heavy disturbed input voltage. The shape of the input voltage during the robustness test can be seen in Fig. 15. At a window size of 150 V no commutation short circuit was measured.

![Change of commutation strategies](image3)

**Fig. 14**: Change of commutation strategies
Introduction

The paper gives a summary of the possible commutation styles and strategies. A new robust commutation strategy without an explicit sign measurement is presented. Measurements of a test set-up running without explicit sign measurement for the first time are shown. The robustness against disturbance is proven by measurements. The new method enables an easy implementation which promises a great reduction in converter expenses. A further milestone in matrix converter design is reached.

References


Fig. 15: Phase-to-phase input voltage during robustness test